INSULATING GATE TYPE FIELD EFFECT TRANSISTOR

Publication number: 53-142189

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1. Title of the invention

Insulating gate type field effect transistor

2. Claim

Insulating gate type field effect transistor comprising: Si substrate consisting of Si base with a first conductive type, a first epitaxial layer having the same conductive type as said first conductive type and higher resistivity than that of said Si base formed onto said Si base, and a second epitaxial layer formed onto said first epitaxial layer having a second conductive type which is opposite to said first conductive type; a netlike diffusion region having a second conductive type formed inside said second epitaxial layer of said Si substrate; a gate oxide formed on the inner surface of a netlike groove which surrounds said diffusion region and whose bottom reaches inside said first epitaxial layer through said second epitaxial layer; a first insulation layer which fills said groove from its bottom to the height above the interface between said first and second epitaxial layers; a gate electrode layer which is formed onto said first insulation layer and whose side wall faces said first epitaxial layer; a second insulation layer which is formed onto said gate electrode layer and fills said groove; a gate electrode electrically connected to said gate electrode layer exposed from a window pierced in a part of said second insulation layer; and a source electrode electrically connected to said diffusion region which is formed and exposed in a netted shape on almost all the surface area of said substrate except the part where said gate electrode is formed.

3. Detailed description of the invention

The present invention relates to an insulating gate type field effect transistor having a vertical structure.

A conventional structure of an insulating gate type field effect transistor (herein after referred to as "MOST") is, for example as shown in Fig.1, a so-called lateral type. In Fig.1, a gate oxide 4 is formed onto a P-type Si substrate 1 located between n-type drain 2 and source 3 regions that are formed in the Si substrate, and furthermore a gate electrode 5 is formed onto the gate oxide. In the lateral type MOST, a current flows in a direction horizontal to a substrate surface through a channel region to be formed underneath the gate oxide 4. However, there are some essential problems in this kind of lateral type MOST, in which a current flows in a direction horizontal to a substrate surface, such as a large current cannot flow, a mutual conductance Gm is small, and neither a high withstand voltage nor a high output can be obtained.

The object of the present invention is to solve the above-mentioned problems involves in the conventional MOST. In the present invention, the above-mentioned problems involved in the lateral type MOST can be solved since a current flows in a direction vertical to a substrate surface by making a structure of MOST vertical and netlike.

The present invention will be explained in detail below with reference to Fig.2 in which the MOST structure of the present invention is shown.

As shown in Fig.2, the MOST of the present invention is comprised of a Si substrate that consists of an N^+-type Si base 6, an N^--type epitaxial layer 7 formed onto the base and a p-type epitaxial layer 8 further formed onto the N^--type epitaxial layer, a netlike N^+-type diffusion region 9 formed inside the p-type epitaxial layer 8 of the Si substrate, a gate oxide 10 formed on the inner surface of a netlike groove which surrounds the

N^+-type diffusion region 9 and whose bottom reaches inside the N^--type epitaxial layer 7 through the p^-type epitaxial layer 8, an insulation layer 11 which fills the groove from its bottom to the height above the interface between the N^--type epitaxial layer 7 and the p^-type epitaxial layer 8, a gate electrode layer 12 which is formed onto the insulation layer 11 and whose side wall faces the p^-type epitaxial layer 8 across the gate oxide 10, an insulation layer 13 which is formed onto the gate electrode layer 12 and fills the groove, a gate electrode 14 electrically connected to the gate electrode layer which is exposed from a window pierced in a part of the insulation layer 13 located near the edge of the Si substrate surface, and a source electrode 15 electrically connected to the N^+-type diffusion region 9 which is formed and exposed in a netted shape on almost all the surface area of the substrate except the part where the gate electrode is formed. In addition, the number 16 in Fig.2 is a p^+-type channel stopper region.

The MOST of the present invention having above-described structure employs the netlike N^+-type diffusion region 9 as a source region, and the N^+-type Si base 6 and N^--type epitaxial layer 7 formed onto the base with its netlike upper part as a drain region. Furthermore, since the gate is located at the side wall of the netlike p^-type epitaxial layer 8 sandwiched between the source and drain regions, the MOST of the present invention has a vertical and netlike structure. In addition, a drain electrode is formed on the whole back surface of the Si substrate.

It is obvious from the above-description that in the MOST of the present invention a channel is formed in a direction vertical to the Si substrate surface and in a netted shape and a current also flows in a direction vertical to the Si substrate surface. Accordingly, a current capacity of the MOST of the present invention is remarkably increased compared with the conventional MOST with a lateral type structure, and therefore a

larger output becomes obtainable. Furthermore, the MOST of the present invention has a structure that can determine its withstand voltage by selecting the values of thickness and resistivity of both N^--type epitaxial layer 7 and p-type epitaxial layer 8. In particular, increasing the resistivity of the N^--type epitaxial layer 7 sufficiently and selecting a large value for its thickness can lead to a higher withstand voltage.

To increase a mutual conductance in a conventional lateral type MOST, shortening a gate length (channel length) by fine pattern processing of the order of 1-2μm is necessary. For such fine pattern processing, comparatively difficult process technology such as UV exposure and EB exposure must be employed and therefore it is difficult to maintain a high processing yield. On the other hand, in the MOST of the present invention, a gate length is determined by the relative relationship between the thickness of the p-type epitaxial layer 8 and the diffusion length of the N^+-type diffusion region, and therefore such a short gate length as obtained by the above-mentioned technology can easily be obtained. Hence, manufacturing the MOST having a large mutual conductance and a large gain with a high yield becomes possible.

As is clear from the above-description, according to the present invention, the MOST having much more superior properties compared with a conventional MOST can be obtained. In addition, although the example of an N-channel type MOST is explained above, it is clear that the present invention is able to apply also to a p-channel type by reversing the conductive type of each region explained above.

4. Brief description of the drawings

Fig.1 is a cross-sectional view showing a structure of a conventional insulating gate type field effect transistor.

Fig.2 is a cross-sectional view showing a structure of an insulating gate type field effect transistor in accordance with one embodiment of the present invention.

6 N^{+}-type Si substrate

7 p^{-}-type epitaxial layer

8 p-type epitaxial layer

9 N^{+}-type diffusion region

10 Gate oxide

11,13 Insulation layer

12 Gate electrode layer

14 Gate electrode

15 Source electrode

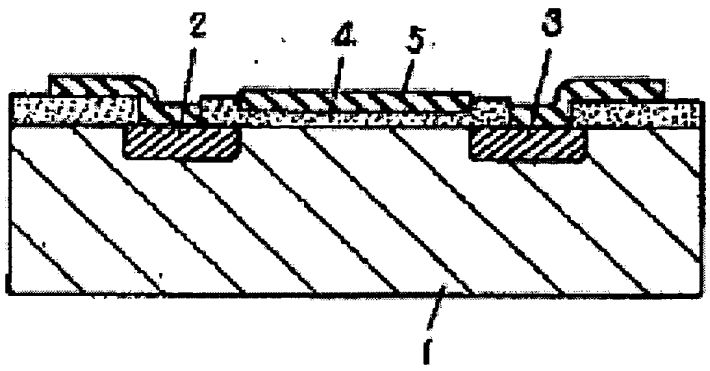

FIG.1

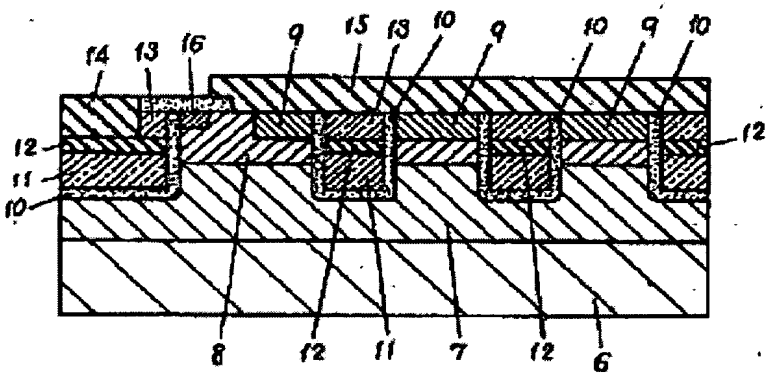

FIG.2

Publication of amendment under the provision of Article 38 (2) of the Patent Law of Japan

Amendment on the patent application number 52-057313 (patent publication number 53-142189, published in the patent gazette number 53-1422 issued on December 11, 1978) is published under the provision of Article 38 (2) of the Patent Law of Japan as follows.

Int. Cl².	Identification symbol	JPO file number
H01L 29/78		6603 5F
29/06		7514 5F
29/60		7638 5F

Amendment

April 8, 1981

Destination: Commissioner of the Patent Office

1 Designation of the case

Patent application number 52-057313

2 Title of the invention

Insulating gate type field effect transistor

3 Party making the amendment

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5 Object for amendment

(1) A "Claim" section in the specification.

(2) A "Detailed description of the invention" section in the specification.

6 Contents of amendment

1 A claim in the specification shall be amended as per enclosure.

2 The term "pattern processing" on page 6, line 3 in the specification shall be amended to "pattern processing".

Claim:

Insulating gate type field effect transistor comprising: Si substrate consisting of Si base with a first conductive type, a first epitaxial layer having the same conductive type as said first conductive type and higher resistivity than that of said Si base formed onto said Si base, and a second epitaxial layer formed onto said first epitaxial layer having a second conductive type which is opposite to said first conductive type; a netlike diffusion region having a second conductive type formed inside said second epitaxial layer of said Si substrate; a gate oxide formed on the inner surface of a netlike groove which surrounds said diffusion region and whose bottom reaches inside said first epitaxial layer through said second epitaxial layer; a first insulation layer which fills said groove from its bottom to the height above the interface between said first and second epitaxial layers; a gate electrode layer which is formed onto said first insulation layer and whose side wall faces said second epitaxial layer; a second insulation layer which is formed onto said gate electrode layer and fills said groove; a gate electrode electrically connected to said gate electrode layer exposed from a window pierced in a part of said second insulation layer; and a source electrode electrically connected to said diffusion region which is formed and exposed in a netted shape on almost all the surface area of said substrate except the part where said gate electrode is formed.